NSS60101DMT

Low $V_{CE(sat)}$ NPN Transistors, 60 V, 1 A

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and LED lightning, power management…etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- NSV60101DMTWTBG − Wettable Flanks Device
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	60	Vdc
Emitter−Base Voltage	V_{EBO}	6	Vdc
Collector Current − Continuous	I_C	1	A
Collector Current − Peak	I_{CM}	2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient (Notes 1 and 2)	$R_{\theta JA}$	55	°C/W
Total Power Dissipation per Package @ T_A = 25°C (Note 2)	P_D	2.27	W
Thermal Resistance Junction−to−Ambient (Note 3)	$R_{\theta JA}$	69	°C/W
Power Dissipation per Transistor @ T_A = 25°C (Note 3)	P_D	1.8	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Dual Operation).
2. P_D per Transistor when both are turned on is one half of Total P_D or 1.13 Watts.
3. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Single−Operation).

ON Semiconductor®

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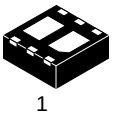
60 Volt, 1 Amp
NPN Low $V_{CE(sat)}$ Transistors



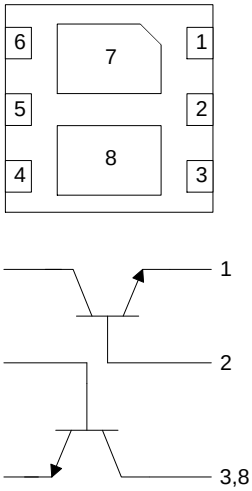
WDFN6
CASE 506AN

MARKING DIAGRAM

AN = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NSS60101DMTTBG	WDFN6 (Pb−Free)	3000/Tape & Reel
NSV60101DMTWTBG	WDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	$V_{(BR)CEO}$	60			V
Collector−Base Breakdown Voltage (Ic = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	80			V
Emitter−Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	6			V
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)	I_{CBO}			100	nA
Emitter Cutoff Current (V_{BE} = 5.0 V)	I_{EBO}			100	nA
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 100 mA, V_{CE} = 2.0 V) (I_C = 500 mA, V_{CE} = 2.0 V) (I_C = 1 A, V_{CE} = 2.0 V) (I_C = 2 A, V_{CE} = 2.0 V	h_{FE}	 150 120 90 35	 250 240 180 55		
Collector−Emitter Saturation Voltage (Note 4) (I_C = 500 mA, I_B = 50 mA) (I_C = 1 A, I_B = 50 mA) (I_C = 1 A, I_B = 100 mA)	$V_{CE(sat)}$		 0.063 0.130 0.115	 0.100 0.200 0.180	V
Base − Emitter Saturation Voltage (Note 4) (I_C = 500 mA, I_B = 50 mA) (I_C = 1 A, I_B = 50 mA) (I_C = 1 A, I_B = 100 mA)	$V_{BE(sat)}$			 1.0 1.0 1.1	V
Base−Emitter Turn−on Voltage (Note 4) (I_C = 500 mA, V_{CE} = 2 V)	$V_{BE(on)}$			0.9	V
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	C_{obo}		10		pF
Cutoff Frequency (I_C = 50 mA, V_{CE} = 2.0 V, f = 100 MHz)	f_T		180		MHz
SWITCHING TIMES					
Delay Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_d		13		ns
Rise Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_r		18		ns
Storage Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_s		700		ns
Fall Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_f		80		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

TYPICAL CHARACTERISTICS

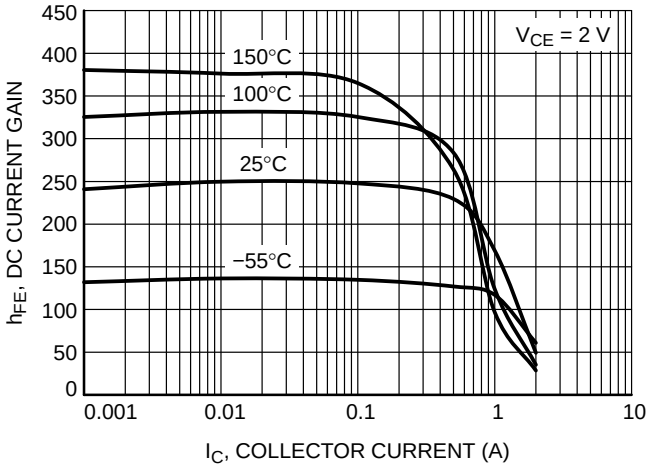


Figure 1. DC Current Gain

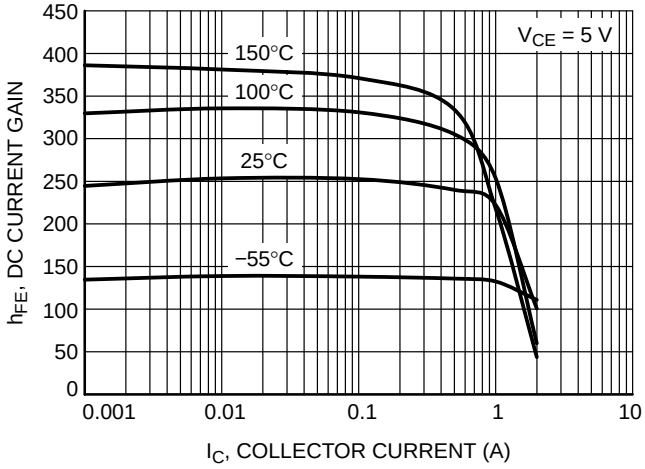


Figure 2. DC Current Gain

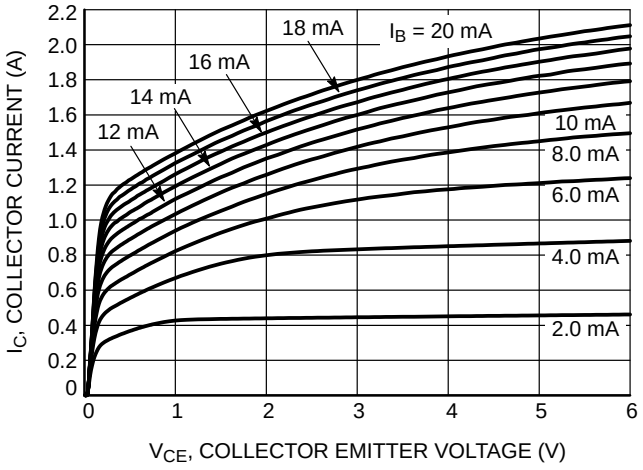


Figure 3. Collector Current as a Function of Collector Emitter Voltage

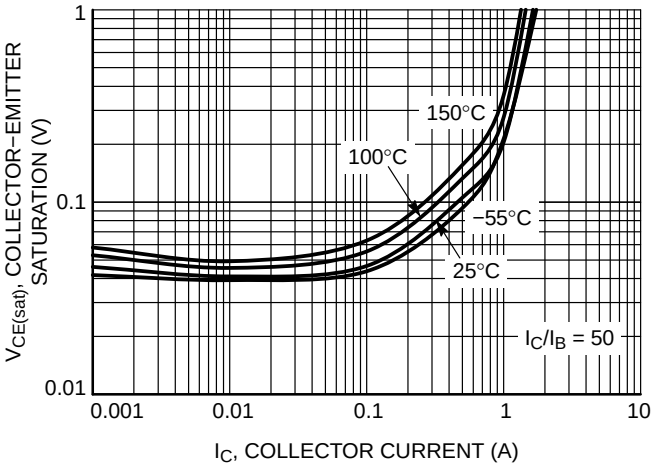


Figure 4. Collector−Emitter Saturation Voltage

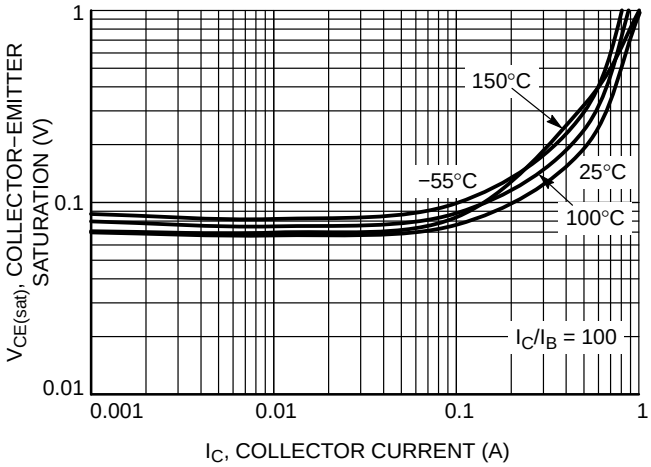


Figure 5. Collector−Emitter Saturation Voltage

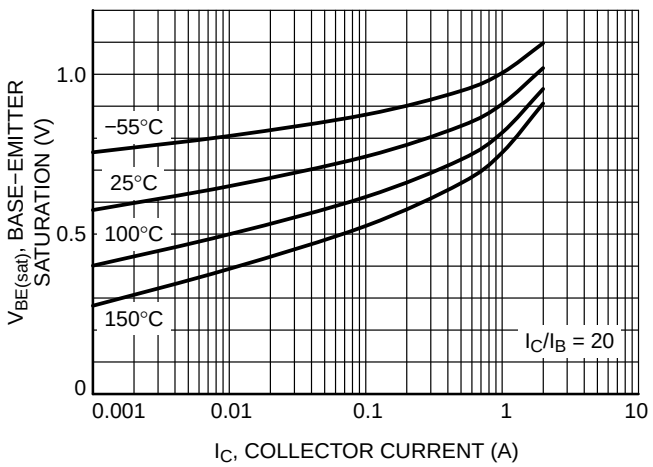


Figure 6. Base−Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

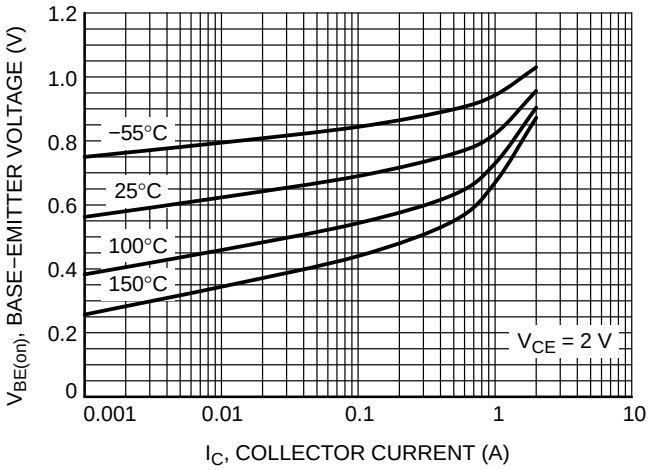


Figure 7. Base−Emitter “ON” Voltage

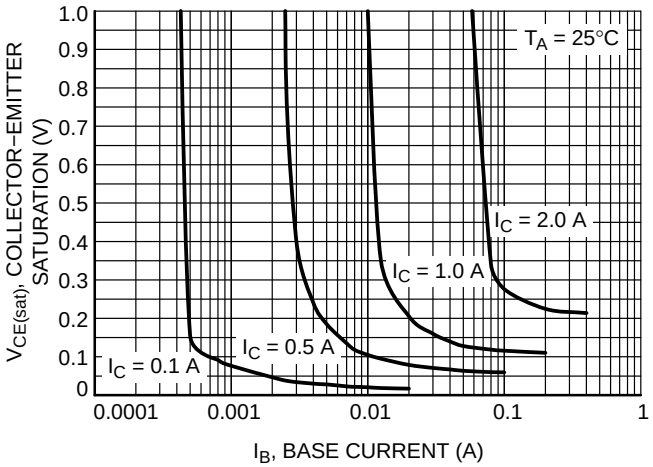


Figure 8. Collector Saturation Region

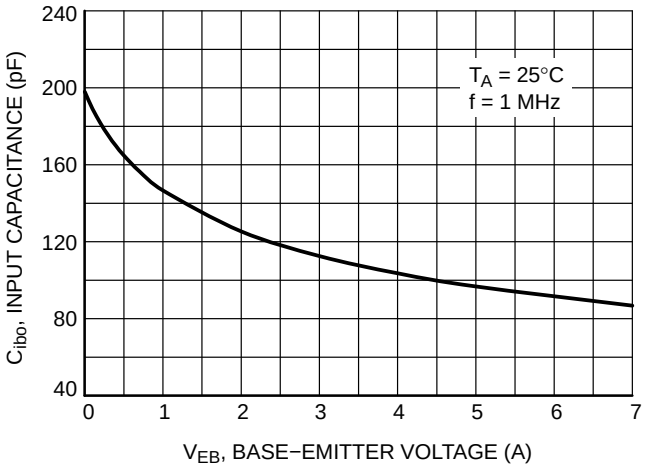


Figure 9. Input Capacitance

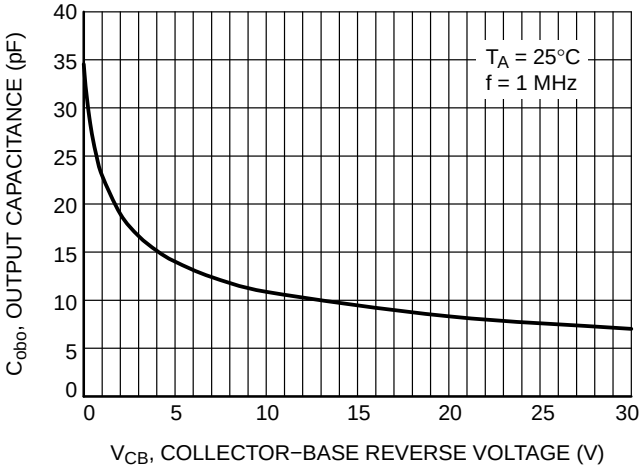


Figure 10. Output Capacitance

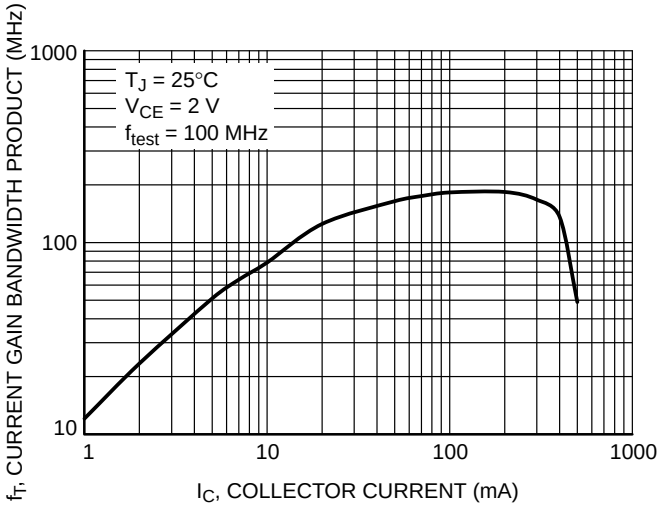


Figure 11. f_T, Current Gain Bandwidth Product

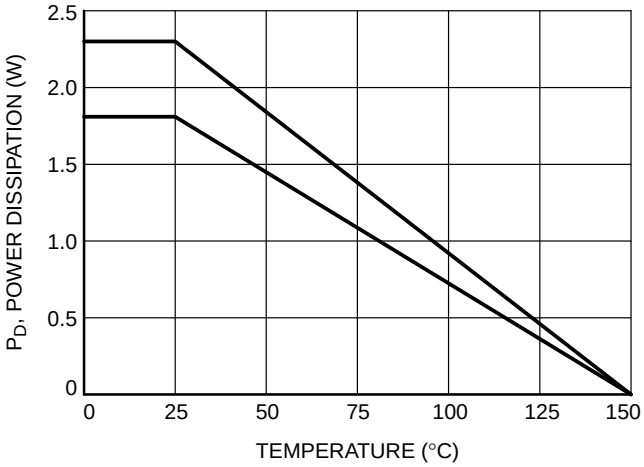


Figure 12. Power Derating

TYPICAL CHARACTERISTICS

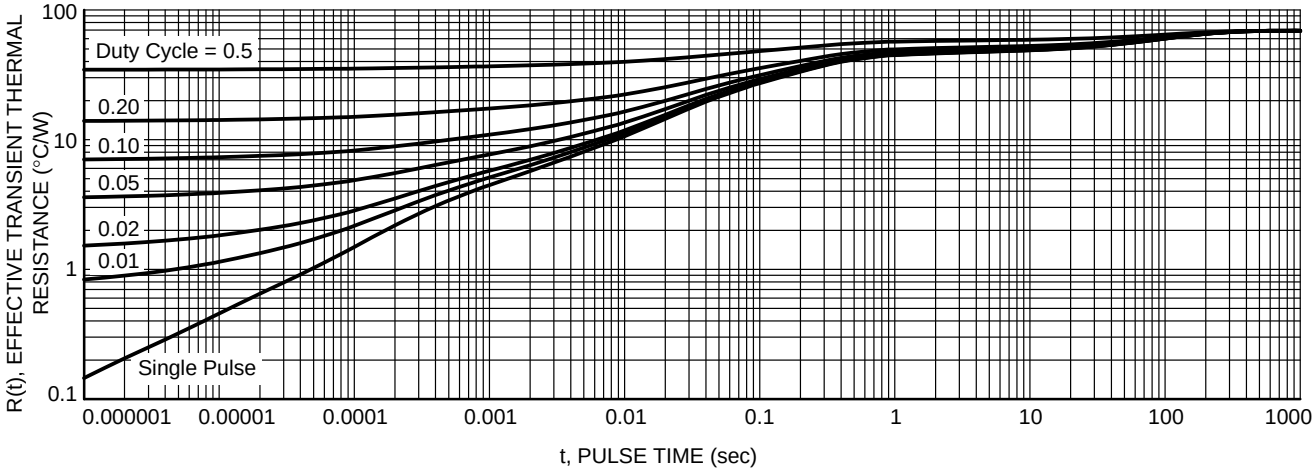


Figure 13. Thermal Resistance by Transistor

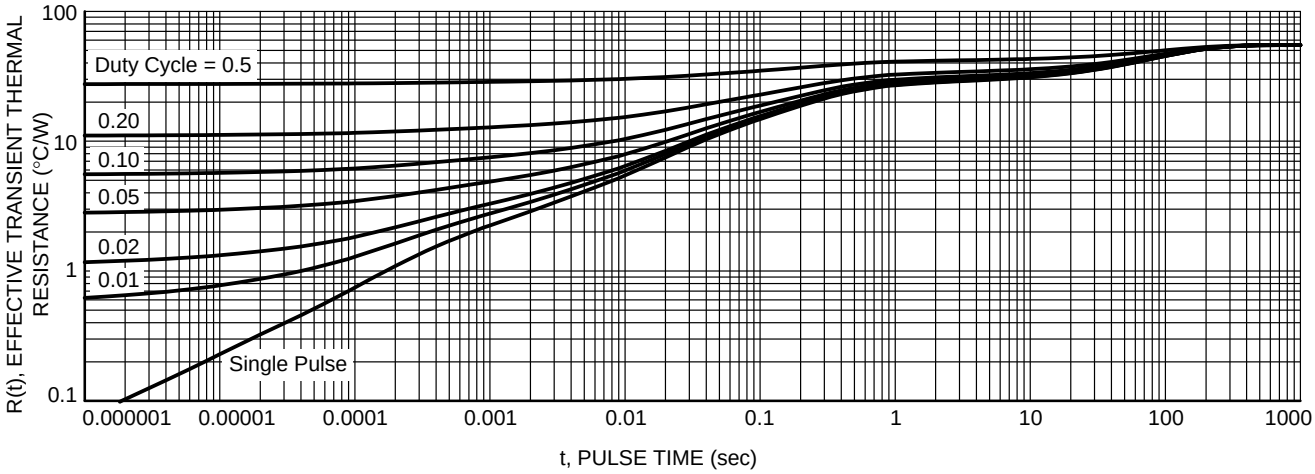


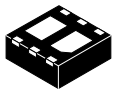
Figure 14. Thermal Resistance for Both Transistors

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

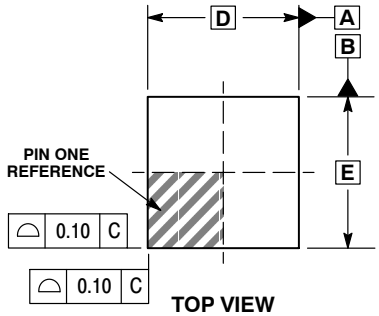
ON Semiconductor®

WDFN6 2x2, 0.65P
CASE 506AN
ISSUE G

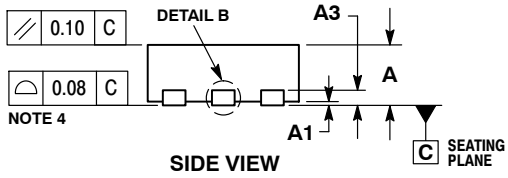
DATE 22 AUG 2013



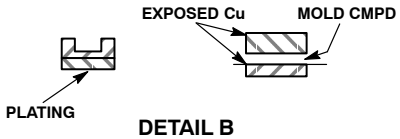
SCALE 4:1



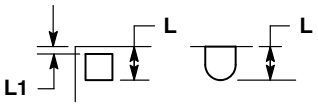
TOP VIEW



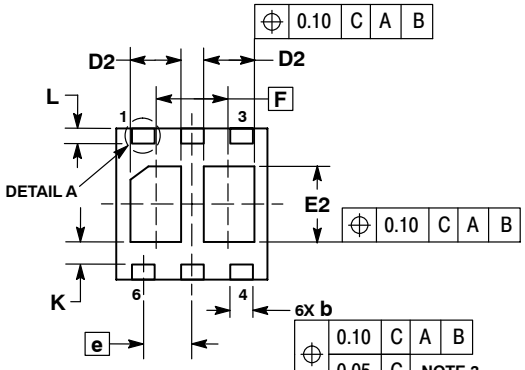
SIDE VIEW



DETAIL B
OPTIONAL CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

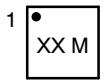


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

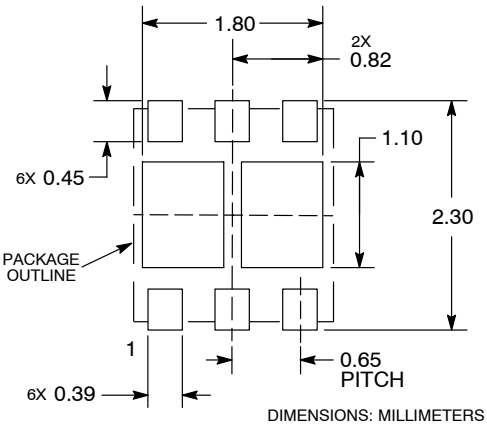
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 2:
PIN 1. ANODE
2. N/C
3. DRAIN
4. SOURCE
5. GATE
6. CATHODE

STYLE 3:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. DRAIN 2
5. GATE 2
6. DRAIN 1

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DESCRIPTION:	**WDFN6 2X2, 0.65P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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